Ahmet Emre Eser

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 Personal Website

EDUCATION

University of California San Diego　　　　　　　　　　　　Sep 2025 - March 2027
M.S. - Electrical and Computer Engineering　　　　　　　　　　　*San Diego, CA*
- Computer engineering track (EC79)

Sabanci University　　　　　　　　　　　　　　　　　　　　May 2025
B.S. - Computer Science and Engineering　　　　　　　　　　　　*Istanbul, Turkey*
- Discontinued dual degree in Electrical Engineering (quit with 1 course to go), GPA: 3.73/4.00
- Assistantships: CS401 - Computer Architecture (Spr 24), CS204 - Advanced Programming (Fall 22)

EXPERIENCE

Sabanci University　　　　　　　　　　　　　　　　　　　Sep 2024 – May 2025
Research Assistant – *DNN Accelerator Architectures*　　　　　　　*Istanbul, Turkey*
- Worked on the design of a DNN training accelerator for the DARTS neural architecture search (NAS) algorithm
- Determined unit specifications based on the existing DARTS software & algorithms
- Designed latency optimized floating point adder & multiplier circuits in *Verilog*, validated in *Verilator*

Ecole Polytechnique Federale de Lausanne (EPFL)　　　　　　June 2024 – Sep 2024
Research Intern – *Datacenter Memory Architectures*　　　　　　*Lausanne, Switzerland*
- Implemented a VA translation on-demand loader/pre-loader for Midgard Virtual Memory Framework in *Chisel*

Analog Devices Integrated (ADI)　　　　　　　　　　　　　Sep 2023 – June 2024
RTL Design Co-Op – *Security/Cryptographic IP Group*　　　　　　*Istanbul, Turkey*
- Implemented NIST compliant elliptic curve digital signature and key exchange operations on hardware in *Verilog*
- Developed elliptic curve digital signature and Diffie-Hellman software for the MAXQ Systems on Chip in *C*
- My work is planned to be implemented **on silicon** in Q1 2027
- Received full time return offer and positive reviews

Analog Devices Integrated (ADI)　　　　　　　　　　　　　June 2023 – Sep 2023
RTL Design Intern – *Security/Cryptographic IP Group*　　　　　　*Istanbul, Turkey*
- Implemented elliptic curve point operations on hardware in *SystemVerilog* for a cryptography coprocessor
- Developed a regression testing script for said elliptic curve cryptography accelerator in *Jenkins*, *Python* & *Bash*
- Optimized area of said elliptic curve cryptography coprocessor
- Received Co-Op conversion offer and positive reviews

Sabanci University　　　　　　　　　　　　　　　　　　　Sep 2023 – Apr 2024
Research Assistant – *Cryptographic Accelerator Architectures*　　　*Istanbul, Turkey*
- RISC-V ISA extension for post quantum cryptography algorithm (Kyber, Dilithium, NTT) acceleration

Tubitak Bilgem National Labs　　　　　　　　　　　　　　Jan 2023 – Feb 2023
Back-end Software Engineering Intern　　　　　　　　　　　　　*Istanbul, Turkey*
- Developed an email microservice for the *Safir-Depo* suite's note taking app using Quarkus and Apache Kafka

PROJECTS

32 bit Operating System for x86 | *C, QEMU, x86 asm*　　　　　　July 2023 - July 2025
Bootloader, VGA drivers, kernel, interrupt tables (IDT, GDT), ISRs, IRQs, kernel

Standard Cell Library for 180nm XFAB PDK | *IC Design, Layout, Cadence Virtuoso*　　　May 2025
Design and layout of serial adder, D latch, D flip flop, full adder, NAND, NOR cells

Adaptive Savitzky-Golay Filter Variant | *Digital Signal Processing, Matlab*　　　　　Apr 2025
Selects window length (M) and polynomial order (p) at every point. Algorithm based on article by John et al.

GPU K-Means Clustering Algorithm Implementation | *Cuda, OpenMP, ML*　　　Dec 2024
Sobel Edge Detection Module for FPGA | *FPGA, Verilog, Computer Vision*　　　May 2023
Bluetooth Environmental Sensing Beacon | *Embedded C, FreeRTOS, Bluedroid, I2C*　　Apr 2023
Interfaces with two I2C sensors, advertises sensor data through Bluetooth Low Energy GAP protocol

SKILLS

Hardware Design: Verilog (fluent), SystemVerilog (intermediate), Chisel (intermediate)
Architectures: RISC-V (knowledgeable), AVR (knowledgeable), MIPS (knowledgeable), ARM (basic), x86 (basic)
Programming Languages: C/C++ (fluent), Python (fluent), Bash (intermediate), CUDA (intermediate)
Tools & Protocols: Cadence Suite, Git, Verilator, QEMU, Vivado, Linux, Makefile, Jenkins, I2C, SPI, FreeRTOS, ns3